

<b>Notice of References Cited</b>	Application/Control No. 10/051,335	Applicant(s)/Patent Under Reexamination TAKAYAMA ET AL.	
	Examiner Satish S. Rampuria	Art Unit 2124	Page 1 of 1

#### U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,559,975 A	09-1996	Christie et al.	712/230
	B	US-5,218,711 A	06-1993	Yoshida, Toyohiko	712/34
	C	US-5,905,893 A	05-1999	Worrell, Frank	717/151
	D	US-5,896,521 A	04-1999	Shackleford et al.	703/21
	E	US-5,179,702 A	01-1993	Spix et al.	718/102
	F	US-6,038,660 A	03-2000	Singh et al.	712/230
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

#### FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

#### NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Chau-Wen Tseng, Compiler optimizations for eliminating barrier synchronization, August 1995, ACM SIGPLAN Notices , Proceedings of the fifth ACM SIGPLAN symposium on Principles and practice of parallel programming, Volume 30 Issue 8, Pages 144-155.			
	V	Lynn et al., Compiler and hardware support for cache coherence in large-scale multiprocessors: design considerations and performance study, May 1996, ACM SIGARCH Computer Architecture News, Volume 24 Issue 2, Pages 283-294			
	W				
	X				

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.